

What is claimed is:

1 1. A pipelined adaptive decision feedback equalizer
2 for equalizing a signal received from a channel, comprising:
3 a pre-processing unit (PP) comprising a plurality of
4 PP coefficients for filtering the signal, and
5 generating a PP output signal;
6 an adder receiving the PP output signal and outputting
7 an added signal;
8 a slicer coupled to the output terminal of the adder,
9 the slicer outputting a decision signal based on
10 the added signal;
11 a feedback filter (FBF) comprising a plurality of FBF
12 coefficients, coupled to the slicer for receiving
13 the decision signal, the feedback filter canceling
14 post-cursor ISI and generating a FBF output
15 signal;
16 a delay unit coupled between the feedback filter and
17 the second input terminal of the adder, the delay
18 unit receiving the FBF output signal and
19 generating the delayed FBF output signal to the
20 adder, wherein the delay unit is a n_1 -tap delay
21 block, n_1 is positive integer and $n_1 \geq 2$;
22 a weight-update block for adapting the FBF coefficients
23 to cancel the post-cursor ISI and selecting a
24 plurality of FBF coefficients from the FBF
25 coefficients; and
26 a mapping circuit for translating the FBF coefficients
27 by a predetermined method to generate the PP
28 coefficients and outputting the PP coefficients

29 to the pre-processing unit, wherein at least one
30 element of the set of the FBF coefficients is
31 different from the corresponding element of the
32 set of the PP coefficients.

1 2. The pipelined adaptive decision feedback equalizer
2 of claim 1, wherein the first weight-update block adapts the
3 coefficients according to a Delay Least-Mean-Square
4 algorithm.

1 3. The pipelined adaptive decision feedback equalizer
2 of claim 1 further comprises:

3 a feedforward filter comprising a plurality of FFF
4 coefficients, coupled between the pre-processing
5 unit and the first input terminal of the adder,
6 the feedforward filter canceling pre-cursor
7 intersymbol interference (ISI) from the PP output
8 signal and generating a FFF output signal to the
9 adder;

10 a second weight-update block for adapting the FFF
11 coefficients to cancel the pre-cursor ISI.

1 4. The pipelined adaptive decision feedback equalizer
2 of claim 3, wherein the second weight-update block adapts
3 the coefficients according to a Delay Least-Mean-Square
4 algorithm.

1 5. The pipelined adaptive decision feedback equalizer
2 of claim 1, wherein, in the mapping circuit, a relation
3 between the third coefficient a_i and the first coefficient
4 b_j is

$$(1 - \sum_{i=1}^M a_i x^i)(1 + \sum_{j=1}^N b_j x^j) = 1 + \sum_{k=1}^{M+N} c_k x^k, \exists c_k = 0 \text{ if } 0 < k < n_1;$$

wherein M is the number of the third coefficient, N is the number of the first coefficient and M, N, i, j and k are positive integers.

6. A decision feedback equalizer for equalizing a signal received from a channel, comprising:

a pre-processing unit (PP) comprising n_1 PP coefficients and a first delay unit, the pre-processing unit filtering the signal, and generating a PP output signal, wherein the first delay unit is a n_1 -tap delay block, n_1 is positive integer and $n_1 \geq 2$;

a feedforward filter (FFF) comprising a plurality of FFF coefficients, coupled to the pre-processing unit to receive the PP output signal, the feedforward filter canceling pre-cursor intersymbol interference (ISI) and outputting a FFF output signal;

an adder having a first input terminal, a second input terminal and an output terminal, the first input terminal coupled to the feedforward filter, the output terminal outputting an added signal;

a slicer coupled to the output terminal of the adder, the slicer outputting a decision signal based on the added signal;

a feedback filter (FBF) comprising n_2 FBF coefficients and a third delay unit, coupled to the slicer, the feedback filter canceling post-cursor ISI and

25 outputting a FBF output signal, wherein the third
26 delay unit is a n_3 -tap delay block, n_2 and n_3 are
27 positive integers and $n_2=n_3+n_1$;
28 a delay unit coupled between the feedback filter and
29 the second input terminal of the adder, the delay
30 unit receiving the FBF output signal and
31 generating a delayed FBF output signal to the
32 second input terminal of the adder, wherein the
33 delay unit is a n_1 -tap delay block;
34 a weight-update block for adapting the FBF coefficients
35 to cancel the post-cursor ISI and selecting n_4 FFF
36 coefficients from the FBF coefficients, wherein n_4
37 is the natural number and $n_4 \geq n_1$; and
38 a mapping circuit for translating the FBF coefficients
39 by a predetermined method to generate the PP
40 coefficients and outputting the PP coefficients to
41 the pre-processing unit, wherein at least one
42 element of the set of the FBF coefficients is
43 different from the corresponding element of the
44 set of the PP coefficients.

1 7. The pipelined adaptive decision feedback equalizer
2 of claim 6, wherein the first weight-update block adapts the
3 coefficients according to a Delay Least-Mean-Square
4 algorithm.

1 8. The pipelined adaptive decision feedback equalizer
2 of claim 6 further comprises:
3 a second weight-update block for adapting the FFF
4 coefficients to cancel the pre-cursor ISI.

1 9. The pipelined adaptive decision feedback equalizer
2 of claim 8, wherein the second weight-update block adapts
3 the coefficients according to a Delay Least-Mean-Square
4 algorithm.

1 10. The pipelined adaptive decision feedback equalizer
2 of claim 6, wherein, in the mapping circuit, a relation
3 between the fourth coefficient a_i and the first coefficient
4 b_j is

5
$$(1 - \sum_{i=1}^M a_i x^i)(1 + \sum_{j=1}^N b_j x^j) = 1 + \sum_{k=1}^{M+N} c_k x^k, \exists c_k = 0 \text{ if } 0 < k < n_1;$$

6 wherein M is the number of the fourth coefficient, N is
7 the number of the first coefficient and M, N, i, j and k are
8 positive integers.